COLD ELECTRONICS STATUS REPORT

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SBND Electronics/DAQ Meeting

September 26, 2016

Intro

- Quick summary of status:
  - FE ASIC
  - ADC ASIC
  - SBND FEMB
- Please see Hucheng's slides in the 9/21 SBND Tech Board meeting (DocDB1300) for more details
- Please see José's talk today for details on Nevis-BNL integration test

FE ASIC

- 240 P1 ASICs delivered to BNL in June
  - Data sheet on SBN DocDB #1196
- P1 changes relative to previous version:
  - Integrate internal pulse generator with 6-bit DAC
  - Increase the buffer-off drive capability of last stage
  - Increase front-end bias current (1nA and 5nA) capability
  - Implement smart reset and increase ESD protection
  - Revise bandgap reference start-up circuit and configuration interface
- Status of tests:
  - DAC characterized with good linearity
  - Buffer-off drive capability increase corrects distortion seen in previous version
  - Additional bias current settings check out
  - Smart reset and revised startup: all ok, no ESD damage or cold startup issues in 30+ chips tested so far

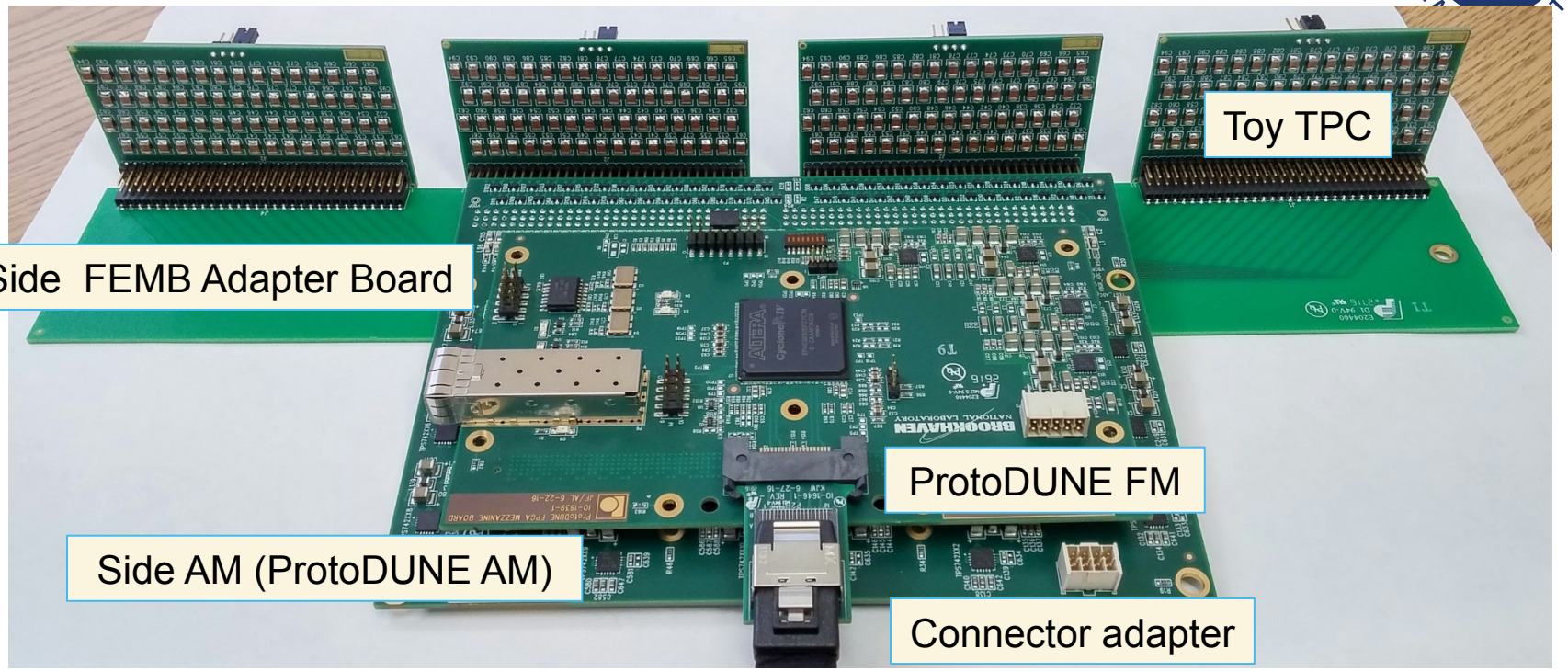
FE ASIC Remaining Issues

- Bias current design glitch
  - Will be corrected in next prototype
  - 1GOhm resistor is needed to bring up all channels
  - An analog mother board with on board bias resistors has been designed and being used in the bench test
- Imperfect pole-zero cancellation
  - Present in previous generation ASICs also: first reported by MSU group with MicroBooNE FE ASICs
  - Imperfect pole-zero cancellation of FE ASIC from MSU can be reproduced at BNL test stand
  - Design change to resolve this problem has been simulated and implemented; will go into next prototype
- Poor linearity and variable baseline observed in P1 ASICs
  - Determined to be due to packaging (no issue observed with bare die)
  - New packaging solutions being investigated

ADC ASIC

- Unpackaged chips received at BNL ~2 weeks ago
- Preliminary tests using bare ASIC and modified test board
  - All channels functions
  - Working at both 1 and 2 MHz
  - First look: significant improvement in stuck codes relative to V*
- Full tests needed for further conclusions

SBND Side FEMB



- Side FEMB Adapter board
  - Passive board with only mating connectors
- Side AM
  - Same size as top AM, only difference is the input mating connector
  - Same design as (Proto)DUNE AM

Tests reveal RC filter works better than LC filter: will be used in final FEMB design